A Universal Coding Approach for Superposition Mapping

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Abstract—Superposition mapping (SM) is a modulation technique that uses linear superposition to produce Gaussian-like data symbols. Communication systems employing SM have a theoretical potential to approach the Gaussian channel capacity without using active signal shaping. This paper tackles several critical issues of SM and provides corresponding solutions. We point out that repetition coding is often an indispensable part for SM systems, a topic which has been obscured for a long time. More importantly, the bandwidth efficiency limit of SM systems with equal power allocation of about 2 bits per symbol per dimension can be eliminated by using irregular repetition codes. Following this cognition, we propose a universal coding approach, called low-density hybrid-check (LDHC) coding, for SM systems with arbitrary power allocation.

I. INTRODUCTION

Considering a linear Gaussian channel, most suitable codes currently available are binary codes, i.e., the code symbols are defined over $GF(2)$. To facilitate physical transmission, one needs to map binary digits onto finite-alphabet symbols that fit with the channel characteristics. According to Shannon [1], the probabilistic distribution of the finite symbol alphabet should be Gaussian-like in order to approach the capacity of linear channels with additive Gaussian noise. Nevertheless, conventional mapping schemes, e.g., amplitude shift keying (ASK), all produce uniformly distributed symbols and are consequently not capacity-achieving. To overcome this problem, signal shaping [2], [3] techniques were proposed to produce symbol sequences with high-dimensional uniform distribution and symbols with low-dimensional non-uniform distribution. In principle, a 1.53 dB ultimate shaping gain can be achieved with an infinite sequence length. However, with modern iteratively decodable codes, the inherent block-wise operation of shaping techniques presents a bottleneck for iterative decoding algorithms which require bit-level reliability informations. In recent years, superposition mapping (SM) starts to attract more and more research interest [4]–[9]. By linearly superimposing binary component symbols, SM is able to deliver a symbol distribution as Gaussian as desired, without the need of an infinite sequence length. Since SM works in a symbol-wise manner, it is compatible with modern iteratively decodable channel codes. For these reasons, SM is considered to be a competent choice for future high-performance systems.

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This paper tackles several open issues of SM. In [6], the high power efficiency of SM with equal power allocation (EPA) is demonstrated. However, a bandwidth efficiency limit of about 2 bits per symbol per dimension is present. A comprehensive discussion on this issue is provided in [8], and it has theoretically been proven that this limit does not come from the mapping scheme but from the code structure that is usually adopted. In this paper, it will be shown that this limit can be easily broken by using an irregular repetition code. Due to the non-bijective non-uniform property of SM-EPA, repetition codes are superior to parity-check codes, which is in contrast with the common understanding. In a coded SM-EPA system, the successful separation of superimposed components mainly rely on the redundancy provided by repetitions. Parity bits are still necessary to improve the system power efficiency and to compensate the unequal error protection effect caused by irregular repetition codes. Nevertheless, the majority of bandwidth expansion should be spent on repetitions instead of parity bits. Given this cognition, we propose a universal coding concept, called low-density hybrid-check (LDHC) code, for SM with any type of power allocation. LDHC coding is a novel way of interpreting SM systems with a serial concatenation of low-density parity-check (LDPC) code and repetition code. The corresponding LDHC matrix enables an all-in-one global-level interleaver design and greatly simplifies the optimization of global-level degree distribution and degree allocation.

II. GAUSSIAN CHANNEL

In this paper, we consider a real-valued additive white Gaussian noise (AWGN) channel, given by

$$y = x + z, \quad z \sim N(0, \sigma_z^2),$$

where $\sigma_z^2 \triangleq N_0/(2E_s)$ is the noise variance. The channel throughput is upper bounded by the mutual information between the input and output:

$$I(x; y) = h(y) - h(y|x) = h(y) - h(z),$$

where $h(\cdot)$ denotes differential entropy. For a given variance the normal distribution maximizes the entropy. Hence, $I(x; y)$ is maximized when $y$ is Gaussian. Normally, the input $x$ is drawn from a finite alphabet, i.e., it is discrete. However, due to the continuous additive noise, $y$ can be made Gaussian when the discrete distribution of $x$ has a Gaussian-like envelope.
be approximated by

\[ H(x) \approx \frac{1}{2} \log(2\pi e N/4) \]  

for large \( N \). Since the symbol entropy upper bounds the mutual information, error-free transmission will only be possible if a channel code with rate \( R \leq H(x)/N \) is applied. Note that \( H(x)/N \) decreases with \( N \) according to (5).

### III. SUPERPOSITION MAPPING

Focusing on one signal dimension, the general structure of superposition mapping is given in Fig. 1. The whole mapping procedure can be mathematically expressed as

\[ x = \sum_{n=1}^{N} c_n = \sum_{n=1}^{N} \alpha_n d_n , \quad d_n \in \{ \pm 1 \} , \]  

(3)

where \( \alpha_n \) is the magnitude of the \( n \)th binary chip \( c_n \), and \( N \) is the bit load of the superposition mapper. Clearly, the set of magnitudes, \( \{ \alpha_1, \alpha_2, \ldots, \alpha_N \} \), specifies the power allocation among superimposed chips. Power allocation significantly influences the supportable bandwidth efficiency and the achievable power efficiency [8]. Among all, superposition mapping with equal power allocation (SM-EPA) presents the biggest challenge for code design. Hence, in this paper we will exclusively focus on SM-EPA.

Equal power allocation (EPA) is the most intuitive yet the most primary power allocation strategy for SM. For EPA, the magnitudes of chips are all identical. That is

\[ \alpha_n = a , \quad 1 \leq n \leq N , \]  

(4)

where \( a \) is a normalization factor to ensure \( E_s = \mathbb{E}\{x^2\} = 1 \). In this case, the superimposed chips \( c_n \) are independent and identically distributed. Consequently, their summation \( x \) tends to be Gaussian distributed if \( N \) is large enough, as demonstrated in Fig. 2. Given a Gaussian-like symbol distribution, the necessity of signal shaping is effectively eliminated. This is verified by the mutual information (MI) curves in Fig. 3. One can see that, without signal shaping, SM-EPA itself is already capacity achieving. Nevertheless, there is a critical issue. It is pointed out in [8] that the entropy of SM-EPA symbols can be approximated by

### IV. CODED SM TRANSMISSION

For \( N > 1 \), SM-EPA is virtually a non-bijective mapping scheme, which works like a lossy source encoder. Even over a noiseless channel, channel coding is still mandatory for SM in order to attain error-free transmission. A schematic diagram of coded SM transmission systems is given in Fig. 4, where DEM stands for superposition demapping. Interleaving is essential for the system performance, as it reduces the mutual dependence among superimposed chips of individual symbols. Later on, we will embed the interleaving functionality into the encoder, when the concept of low-density hybrid-check codes is presented.

Given the channel output and the a priori information from the decoder, the superposition demapper needs to provide soft decisions for each coded bit. In general, a soft-in soft-out APP demapper computes the extrinsic log-likelihood ratio

\[ \text{LLR}(b_n) = \ln \frac{p(y|b_n = 0)}{p(y|b_n = 1)} = \ln \frac{\sum_{b_{\sim n}} p(y|b_{\sim n} = 0, b_n) P(b_{\sim n})}{\sum_{b_{\sim n}} p(y|b_{\sim n} = 1, b_n) P(b_{\sim n})} \]  

(6)

where \( b_{\sim n} \in [b_1, b_2, \ldots, b_{n-1}, b_{n+1}, \ldots, b_N] \)

(7)

denotes the set of code bits excluding \( b_n \). Note that

\[ P'(b_{\sim n}) = \prod_{i=1, i\neq n}^{N} P(b_i) \]  

(8)

due to the statistical independence of interleaved code bits. A verbatim implementation of the above computation involves a complexity proportional to \( N2^N \). However, by using the BCJR algorithm [10] and the tree representation proposed in [6], the demapping complexity can be reduced to \( N^2 \) without any performance loss.
V. REPETITION VS. PARITY BITS

The key task of channel coding is to introduce redundancy to the originally independent information bits. Without loss of generality, the way of adding redundancy can be categorized into two classes: repetition and parity bits. Conventionally, the latter is favorable, since it brings coding gain. For systems with bijective uniform mapping schemes, e.g., ASK, the only task of channel coding is to combat the additive noise. Now, with a non-bijective non-uniform mapping scheme, the situation becomes different. For systems employing SM-EPA, the primary task of channel coding is to ensure a perfect separation of superimposed chips, while combating the additive noise becomes the secondary task. We will show that repetition is much more efficient than parity bits for the first task. Meanwhile, parity bits are still necessary because of the second task.

Consider SM-EPA transmission over a noiseless channel. For simplicity, let \( N = 2 \). The corresponding mapping rule is given in Fig. 5. There are four possible inputs but only three possible outputs. Given i.u.d. input bits, we have \( P_2(0) = 1/2 \) and \( P_2(\pm 2) = 1/4 \). At the initial iteration, there is no a priori information available. Hence, the APP demapper delivers

\[
\text{LLR}(b_1) = \text{LLR}(b_2) = \begin{cases} 
0 & \text{if } y = 0, \\
\pm \infty & \text{if } y = \pm 2.
\end{cases}
\]  

(9)

Note that the event \( \{ y = 0 \} \) occurs with probability 1/2. Thereby, in the demapper outputs, half of the bits are virtually erased. For larger \( N \), the situation becomes more complicated. However, it is easy to imagine that the demapper outputs at the initial iteration have a very large dynamic range. Besides, a big portion of the outputs are either zero or close to zero. Now, with such low-quality soft inputs, the decoder needs to generate meaningful feedbacks to facilitate further iterations. This is indeed not easy for parity-check codes.

Parity checks are in general sensitive to the dynamic range of the inputs. Let \( L_i^{(I)} \) and \( L_i^{(O)} \), \( i = 1, 2, \ldots, D \), denote the input and output LLRs of a degree-\( D \) parity check. We have

\[
L_i^{(O)} = \bigoplus_{1 \leq j \leq D, j \neq i} L_j^{(I)} \approx \min_{1 \leq j \leq D, j \neq i} |L_j^{(I)}|,
\]

where \( \bigoplus \) is the box-plus operator [11]. As long as one input I-value is close to zero, the parity check will fail to generate meaningful extrinsic outputs. Consequently, purely parity-check-based channel codes have a big problem to work with SM-EPA. Illustrated in Fig. 6, for a moderate bit load of \( N = 6 \), a rate 1/8 regular LDPC code is still not able to open the tunnel for convergence, even over a noiseless channel.

As long as one input L-value is strong, the decoder will generate meaningful feedbacks, which is in sharp contrast to parity-check codes. This property is indeed very desirable for an SM-EPA demapper. Consequently, one expects a better situation for repetition-coded SM-EPA. According to the EXIT chart analysis [12], [13] provided in Fig. 6, this conjecture is true. A rate 1/3 repetition code already opens the convergence tunnel for SM-EPA with \( N = 6 \). Furthermore, there is an interesting phenomenon. A rate 2/N repetition code is almost always at the edge of opening the convergence tunnel. This well explains the previously known bandwidth efficiency limit of about 2 bits per symbol per dimension reported in many previous works [6], [14], [15]. However, this limit does not come from SM-EPA itself but from the improperly matched channel code, which can be seen by checking the top value of MI curves in Fig. 3. Now, with irregular degree distribution, a rate 1/7 repetition code can already widely open the convergence tunnel for \( N = 16 \), as shown in Fig. 6. Given this setup, the achieved throughput is \( RN \approx 2.3 \) bits/symbol. The results in Fig. 7 verifies the effectiveness of this design. Note that an irregular degree distribution also shortens the distance to the channel capacity, because of improved decoding threshold. Nevertheless, there is still a non-trivial distance to the capacity. To further reduce this distance, one needs some parity bits to improve the efficiency of information spreading.
VI. LOW-DENSITY HYBRID-CHECK CODE

From the former discussions, we see that repetition is very efficient in enabling the separation of superimposed chips. Nevertheless, parity bits are still necessary to spread information in a more bandwidth-economic way. Therefore, a good coding scheme for SM-EPA should consist of both repetitions and parity bits, though the majority of bandwidth should be spent on repetitions. For this reason, we propose a versatile coding concept, called low-density hybrid-check (LDHC) coding, to facilitate the corresponding code design.

A. Principle & Property

An intuitive approach to add repetitions as well as parity bits is to use a serial concatenation of low-density parity-check (LDPC) code [16], [17] and repetition code, as depicted in Fig. 8(a). Due to its robustness, this type of code structure is commonly adopted in interleave-division multiple-access (IDMA) systems [5], [18], [19], which are in fact another type of superposition systems. Typically, the attention of code optimization is paid to the outer LDPC code [20], while the inner repetition code is rarely considered. From Sec. V, we see that the degree distribution of repetition code significantly influences the supportable bandwidth efficiency as well as the decoding threshold. Therefore, to have optimal performance, the repetition code should also be included in the code design. Moreover, the outer parity-check code and the inner repetition code should be optimized jointly instead of separately.

Fig. 8(b) shows a factor graph representation of an SM system with serially concatenated parity-check code and repetition code. Filled squares denote channel observations. Circled additions denote summation checks, i.e., superposition mapping nodes. Blank circles represent variable nodes, and boxed additions stand for parity checks. Effectively, the variable nodes correspond to the code bits at the output of the LDPC encoder. By linking multiple summation checks to each individual variable node, the repetition code and the interleaver are both included in this factor graph. Hence, it is a general graph for the complete transmission system under consideration. As a matter of fact, this general graph can be fully described by a single incidence matrix, to be explained in the following.

Illustrated in Fig. 9, the incidence matrix consists of two parts. Each row in the upper part corresponds to a summation check, while each row in the lower part corresponds to a parity check. Each column corresponds to one code bit, and each nonzero entry marks the association of a particular code bit with a certain summation/parity check. Unlike in LDPC codes, now the variable nodes have no direct connection to the channel. Instead, the results of summation checks are transmitted over the channel. Certainly, given a reasonable block length, this matrix will be of low density. Since this incidence matrix comprises two different type of code checks, we may call it low-density hybrid-check matrix. Effectively, the upper part of the matrix describes a low-density summation-check (LDSC) code and the lower part corresponds to a low-density parity-check code. Given this all-in-one incidence matrix, the task of code design can be accomplished via matrix construction subject to certain constraints. Clearly, all the available methods from LDPC code design can be easily borrowed, e.g., the MacKay method [21], the PEG/ACE algorithms [22], [23], and the finite-geometry method [24].

Without loss of generality, short cycles should be avoided, particularly length-4 cycles. Short cycles prevent an iterative receiver to converge to the maximum-likelihood solution. To eliminate length-4 cycles, one needs to guarantee that no two columns (or two rows) have more than one 1 in common. Note that doing so (to an LDHC matrix) eliminates short cycles in a global level, i.e., no summation checks will form short cycles, no parity checks will form short cycles, and no summation checks will form short cycles with parity checks. Hence, an LDHC matrix enables a global-level interleaver optimization.

Another benefit of using LDHC matrices is that a global-level optimization of the degree distribution of variable nodes now becomes possible, which is later explained via a simple example. Related methods from LDPC code design, such as density evolution [25] and curve fitting [13], can also be used here. In addition to degree distribution, there is an additional issue for the LDHC codes: degree allocation. Degree allocation determines the portion of repetitions that are assigned to the upper part and lower part of the LDHC matrix, respectively. This is to balance the bandwidth expansion among parity-check code and repetition code. Note that repetitions in the upper part of the LDHC matrix are true repetitions, which are bandwidth-expensive, while those in the lower part are virtual repetitions, which are bandwidth-economic.
nodes is properly adjusted.

The discussion is exclusively focused on SM-EPA, the LDHC code, is proposed to enable a unified code design. Though

A novel concept, called low-density hybrid-check (LDHC) employing superposition mapping (SM). It is pointed out that a

allocation, one expects further improvements.

With optimized degree distribution and degree

2

is provided for code bits with true repetition degree

⩾ 1

Parity checks are exclusively assigned to those code bits

and schematic. With optimized degree distribution and degree

v1 = 10

E

100 iterations, 460000 symbols per burst.

B. Code Design Example

There are many ways to design an LDHC code. We provide here a heuristic example. Suppose that the targeted information rate is 2 bits/symbol. Checking Fig. 3, one will find that SM-EPA with \( N = 8 \) suffices this requirement. We start with a regular rate 1/4 repetition code, i.e., without parity bits. In Fig. 10, you can see that the Turbo cliff appears around \( E_b/N_0 = 8 \) dB. Since the decoding threshold is primarily determined by the true repetitions, we first need to vary the degree distribution of the true repetitions in order to obtain a potential gain. With the following degree distribution

\[
0.18D^1 + 0.31D^4 + 0.50D^5 + 0.01D^8.
\]

the decoding threshold is improved, albeit with a degraded slope and a non-trivial error floor. Then, we remove a few true repetitions to make room for parity bits, by taking

\[
0.25D^3 + 0.31D^4 + 0.43D^5 + 0.01D^8.
\]

The coding rate of the repetition code is increased to 25/93. Utilizing the saved bandwidth, we now apply a rate 93/100 LDPC code with variable node degree distribution

\[
0.06D^3 + 0.19D^2 + 0.75D^0.
\]

Parity checks are exclusively assigned to those code bits with degree-1 true repetition. That is, no further protection is provided for code bits with true repetition degree \( \geq 4 \). Demonstrated in Fig. 10, the resulting performance is about 2.5 dB away from the Shannon limit (for Gaussian inputs) at \( P_b = 10^{-4} \). Note that this code design is rather coarse and schematic. With optimized degree distribution and degree allocation, one expects further improvements.

VII. CONCLUSION

This paper investigates suitable channel codes for systems employing superposition mapping (SM). It is pointed out that a repetition code is often an indispensable part for SM systems. Via irregular repetition codes, the bandwidth efficiency of SM systems with equal power allocation (EPA) can be improved. A novel concept, called low-density hybrid-check (LDHC) code, is proposed to enable a unified code design. Though the discussion is exclusively focused on SM-EPA, the LDHC code is actually universal for SM with arbitrary type of power allocation, given that the degree allocation of the variable nodes is properly adjusted.

REFERENCES